AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A semiconductor structure comprising a high performance metal stacked inductor having a relatively low sheet resistance, said metal stacked inductor comprising at least one first layer of metal which serves as an upper metal wire in the semiconductor structure and a second layer of metal located directly on top of the first layer of metal, wherein said first layer of metal is in electrical contact with a lower metal wire by a via, and said first layer of metal and said second layer of metal are not interconnected by a via.

2. (Previously Presented) The semiconductor structure of Claim 1 further comprising a third metal layer located directly on top of the second layer of metal, wherein said second layer of metal and said third layer of metal are not interconnected by a via.

3. (Original) The semiconductor structure of Claim 1 wherein the metal stacked inductor is spiral shaped.

4. (Original) The semiconductor structure of Claim 2 wherein the metal stacked inductor is spiral shaped.

5. (Original) The semiconductor structure of Claim 1 wherein the first layer of metal is connected to a lower metal wiring level.

6. (Original) The semiconductor structure of Claim 5 wherein said lower metal wiring level comprises a wiring region embedded within an interconnect dielectric.

7. (Previously Presented) The semiconductor structure of Claim 2 further comprising at least one wiring region that lies to the periphery of the metal stacked inductor, wherein in the at least one wiring region the second layer of metal serves as a via interconnecting two metal wires.

8. (Original) The semiconductor structure of Claim 1 wherein the first layer of metal is comprised of a low resistivity conductive material having a resistivity of about 3.0 micro-ohm*cm or less.

9. (Original) The semiconductor structure of Claim 8 wherein the low resistivity conductive material is selected from the group consisting of Cu, Al, Pt, Ag, Au, and alloys thereof.

10. (Original) The semiconductor structure of Claim 8 wherein the low resistivity conductive material is Cu.

11. (Original) The semiconductor structure of Claim 1 wherein the second layer of metal is comprised of a low resistivity conductive material having a resistivity of about 3 micro- ohm*cm or less, said second layer of metal comprising the same or different conductive material as the first layer of metal.

12. (Original) The semiconductor structure of Claim 11 wherein the low resistivity conductive material is selected from the group consisting of Cu, Al, Pt, Ag, Au, and alloys thereof.

13. (Original) The semiconductor structure of Claim 11 wherein the low resistivity conductive material is Al or Cu.

14. (Original) The semiconductor structure of Claim 2 wherein the third layer of metal is comprised of a low resistivity conductive material having a resistivity of about 3 micro- ohm*cm or less, said third layer of metal comprising the same or different conductive material as the first or second layers of metal.

15. (Original) The semiconductor structure of Claim 14 wherein the low resistivity conductive material is selected from the group consisting of Cu, Al, Pt, Ag, Au, and alloys thereof.

16. (Original) The semiconductor structure of Claim 14 wherein the low resistivity conductive material is Al.

17. (Original) The semiconductor structure of Claim 1 wherein the first layer of metal is comprised of Cu and the second layer of metal is comprised of Al.

18. (Original) The semiconductor structure of Claim 2 wherein the first layer of metal is comprised of Cu, the second layer of metal is comprised of Cu and the third layer of metal is comprised of Al.

19. (Currently Amended) A method of forming a semiconductor structure comprising:

providing a partial interconnect structure comprising a lower metal wiring level located on a substrate;

forming a first dielectric material on the partial interconnect structure;

forming a first layer of metal in said first dielectric material, said first layer of metal serves as an upper metal wire of the interconnect structure and as the bottom layer of a metal stacked inductor, wherein said first layer of metal is in electrical contact with a lower metal wire by a via; and

forming a second layer of metal on said first metal layer, wherein said first layer of metal and said second layer of metal are not interconnected by a via.

20. (Previously Presented) The method of Claim 19 further comprising forming a third layer of metal directly on top of the second layer of metal, wherein said second layer of metal and said third layer of metal are not interconnected by a via.